**In the Claims:**

Please cancel claims 2-3, 8, 11, and 19. Please amend claims 1, 7, and 12. The claims are as follows:

1. (Currently amended) A memory array comprising a compilable address magnitude comparator, the compilable address magnitude comparator receiving a self-test address from a self-test controller and comparing the self-test address to a compiled maximum address of the memory array, the compilable address magnitude comparator preventing testing of memory of the memory array corresponding to the self-test address if the self-test address exceeds the compiled maximum address, wherein the compilable address magnitude comparator prevents testing of memory of the memory array by forcing a memory pass signal, wherein the compilable address magnitude comparator includes a row comparator and a column comparator, the row comparator comparing a self-test row address of the memory array and the column comparator comparing a self-test column address of the memory array, and wherein the compiled maximum address comprises a maximum row address of the memory array and a maximum column address of the memory array.

2-3. (Canceled)

4. (Previously presented) The memory array of claim 1, wherein the compilable address magnitude comparator prevents testing of memory of the memory array by forcing a read

operation instead of a write operation.

5-6. (Canceled)

7. (Currently amended) A memory array comprising a compilable address magnitude comparator, the compilable address magnitude comparator comprising:

a row comparator, the row comparator comparing a row portion of a self-test address from a self-test controller with a compiled maximum row address, the compiled maximum row address corresponding to a maximum valid row address of the memory array; and

a column comparator, the column comparator comparing a column portion of the self-test address with a compiled maximum column address, the compiled maximum column address corresponding to a maximum valid column address of the memory array, and wherein the compilable address magnitude comparator modifies a self-test operation of the memory array when either the row portion of the self-test address exceeds the corresponding maximum valid row address or the column portion of the self-test address exceeds the corresponding maximum valid column address, wherein the compilable address magnitude comparator prevents testing of memory of the memory array by forcing a memory pass signal in a corresponding built-in-self-test controller, wherein the compilable address magnitude comparator prevents testing of memory of the memory array by forcing a read operation instead of a write operation, and wherein the row comparator includes at least one logic block selected from a plurality of logic blocks, with each of the plurality of logic blocks corresponding to a portion of a compiled maximum address of the memory array such that by selecting one of the plurality of logic blocks, the compilable magnitude comparator tests for the compiled maximum address of the memory array.

8-11. (Canceled)

12. (Currently amended) An application specific integrated circuit, the application specific integrated circuit comprising:

a memory array comprising a compilable address magnitude comparator;

a built-in-self-test controller, the built-in-self-test controller testing the memory, the compilable address magnitude comparator receiving a self-test address from the built-in-self-test controller and comparing the received self-test address with a compiled maximum address of the memory array, wherein the compiled maximum address corresponds to the highest valid address for the memory array, and wherein the compilable address magnitude comparator prevents the built-in-self-test controller from testing a memory location of the memory array corresponding to the self-test address if the self-test address exceeds the compiled maximum address, wherein the compilable address magnitude comparator prevents testing of memory by forcing a read operation instead of a write operation, and wherein the compilable address magnitude comparator prevents testing of memory by further forcing a memory pass signal, and wherein the second memory array has a different maximum number of columns than does the first memory array.

13. (Previously presented) The application specific integrated circuit of claim 12, wherein the compilable address magnitude comparator includes a row comparator and a column comparator,

the row comparator comparing a self-test row address and the column comparator comparing a self-test column address.

14. (Previously presented) The application specific integrated circuit of claim 13, wherein the compiled maximum address comprises a maximum row address of the memory array and a maximum column address of the memory array.

15. (Previously presented) The application specific integrated circuit of claim 12, wherein the compilable address magnitude comparator prevents testing of memory by forcing a read operation instead of a write operation.

16. (Canceled)

17. (Previously presented) The application specific integrated circuit of claim 12, further comprising:

a second memory array that includes a second compilable address magnitude comparator, the compilable address magnitude comparator receiving self-test address from the built-in-self-test controller and comparing the received self-test address with a second compiled maximum address, wherein the second compiled maximum address corresponds to the highest valid address for the second memory array, and wherein the compilable address magnitude comparator prevents the built-in-self-test controller from testing a memory location in the second memory array corresponding to the self-test address if the self-test address exceeds the second compiled maximum address.

18. (Previously presented) The application specific integrated circuit of claim 17, wherein the second memory array has a different size than the first memory array.

19. (Canceled)

20. (Previously presented) The application specific integrated circuit of claim 12, wherein the comparator is compilable by selectively substituting a plurality of compilable logic blocks according to the compiled maximum address.